FIG.1

11
6
8
C
9
A
B
A
B
BL
4
C
9
WL

FIG.2

section A-A

4;floating gate

11;control gate

9
16
3
15
1
N   N
P
9;device isolation
shielding electrode
2
8;source region
6;drain region

FIG.3

section B-B

FIG.4

section C-C

FIG.5

FIG.6A

section A-A

14

13 ;first polysilicon film

3

P

1

FIG.6B

section B-B

14

13

3

P

1

FIG.6C

section C-C

14

13

3

P

1
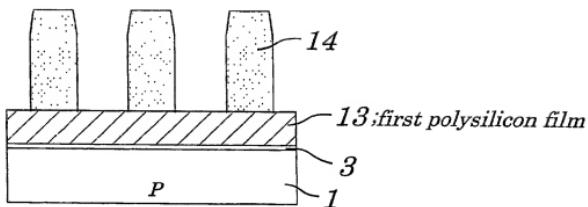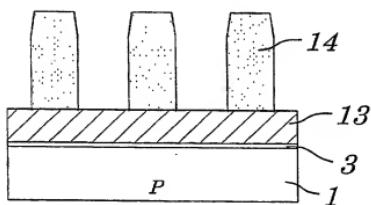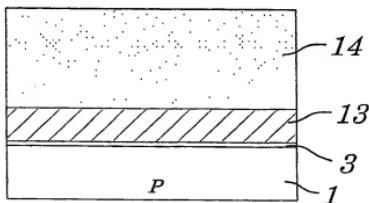
FIG. 7A
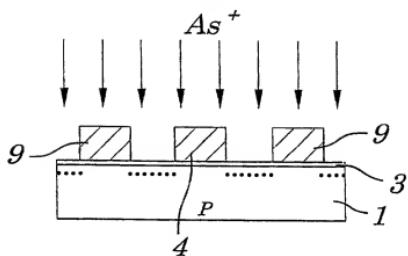
section A-A

FIG. 7B

section B-B
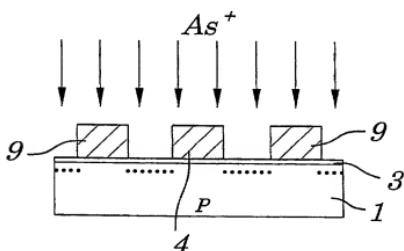
FIG. 7C

section C-C
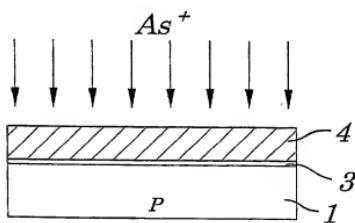
FIG.8A
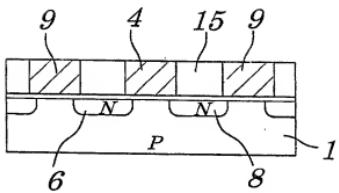
section A-A

FIG.8B

section B-B
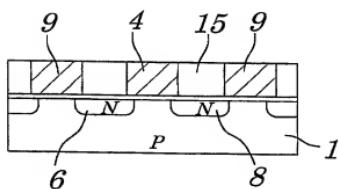

FIG.8C

section C-C
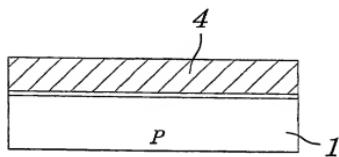
FIG.9A

section A-A

9 4 9 16
N N
6 P 8 1

FIG.9B

section B-B

9 4 9 16
N N
6 P 8 1

FIG.9C

section C-C

16
4
P 1

FIG.10A

section A-A

18 4 17;second polysilicon film
16
9 9
N N
P
6 8 1

FIG.10B

section B-B

18 4 17
16
9 9
N N
P
6 8 1
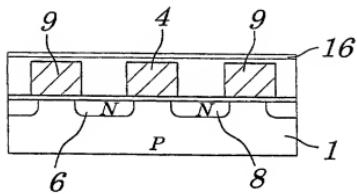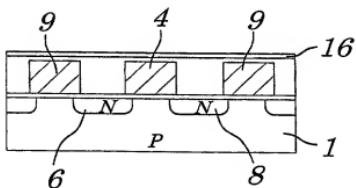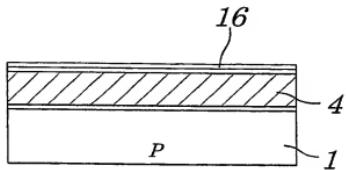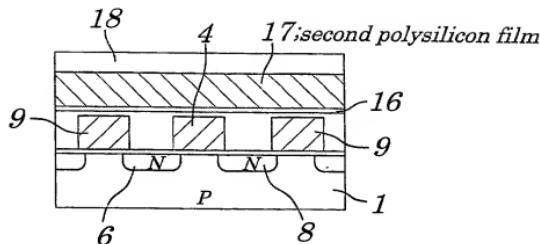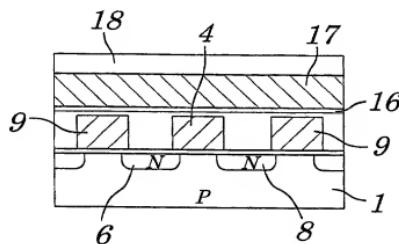
FIG.10C

section C-C

18 17
16
4
P 1
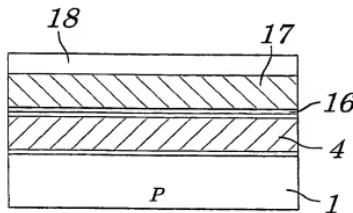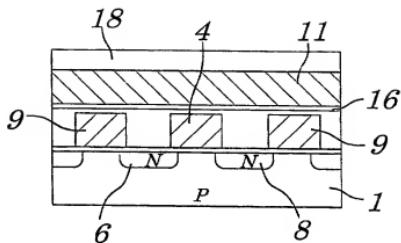
FIG.11A

section A-A

FIG.11B

section B-B
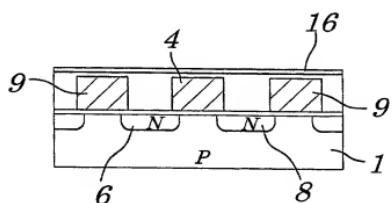
FIG.11C

section C-C
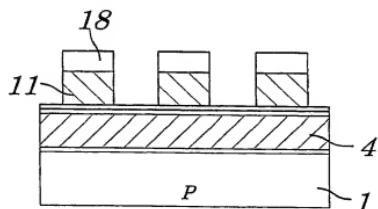
FIG.12A

section A-A
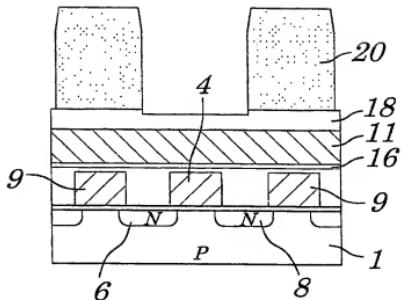

FIG.12B

section B-B
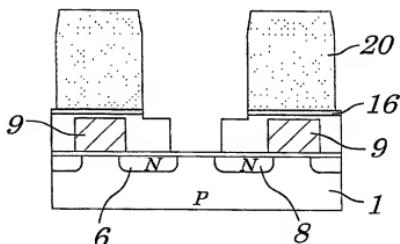
FIG.12C

section C-C

FIG.13

11
8
9
6
C
A
A
B
B
BL
24
C
9
WL

FIG.14

section A-A

24;upper floating gate

4
11
16
21
15
9
9
3
N
N
1
P
6
2
8
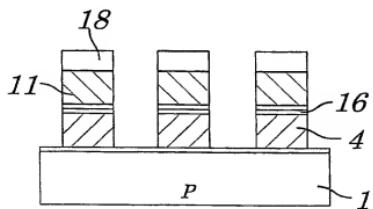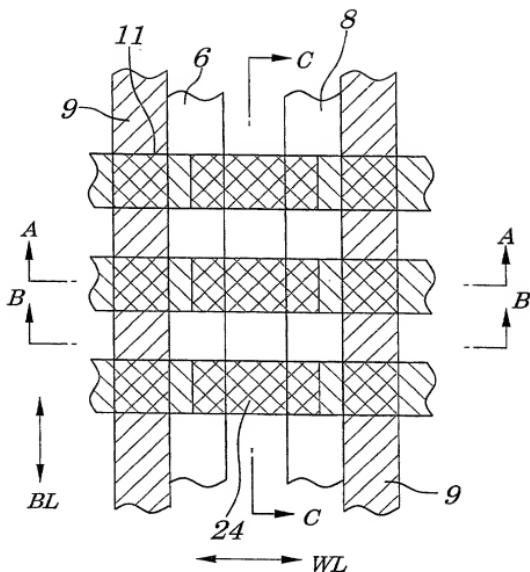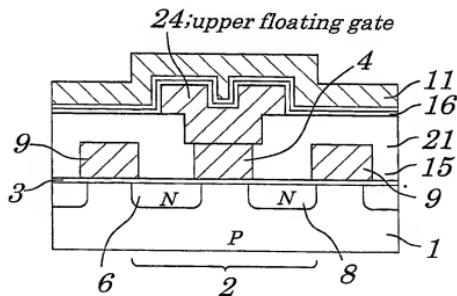
FIG.15
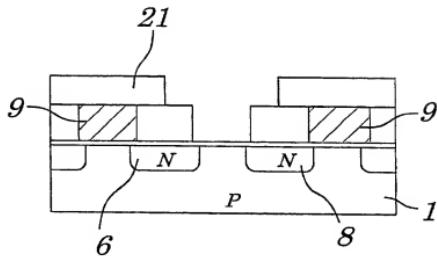
section B-B

FIG.16

section C-C

FIG.17

FIG.18A

section A-A
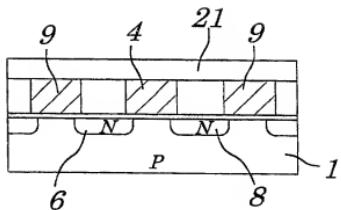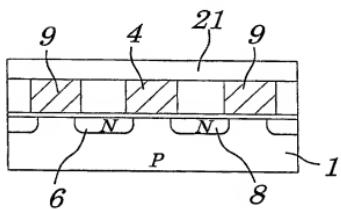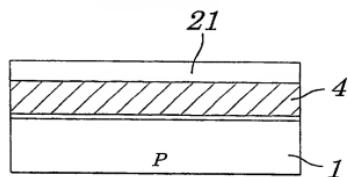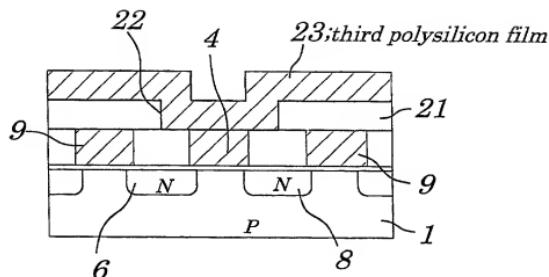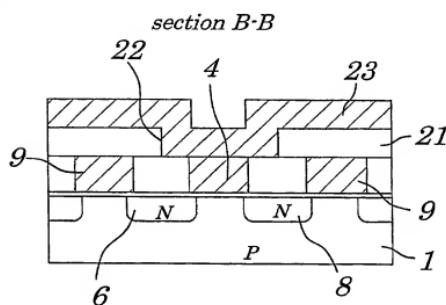
9 4 21 9

N N

P

6 8

1

FIG.18B

section B-B

9 4 21 9

N N

P

6 8

1

FIG.18C

section C-C

21

4

P

1

FIG.19A

section A-A

22 4 23;third polysilicon film

21

9

9

N N

P

6 8 1

FIG.19B

section B-B

22 4 23

21

9

9

N N

P

6 8 1

FIG.19C

section C-C

23

4

P 1

FIG.20A section A-A

24
11
16
21
9
9
N   N
P
1
6   4   8

FIG.20B section B-B

21
9   9
N   N
P
1
6   8

FIG.20C section C-C

11
24
16
4
P
1

FIG.21

FIG.22

section A-A

4A;first floating gate

8

4B;second floating gate
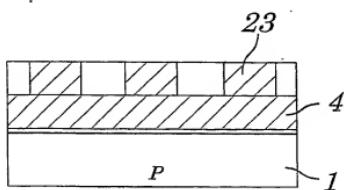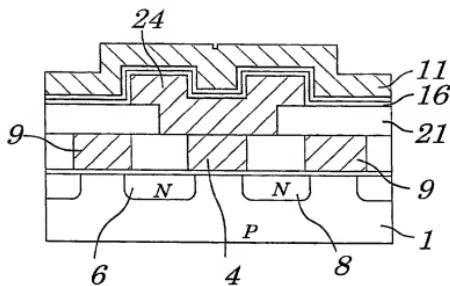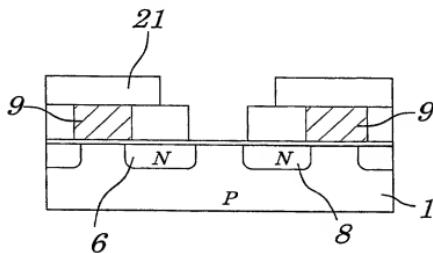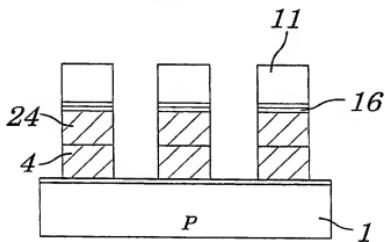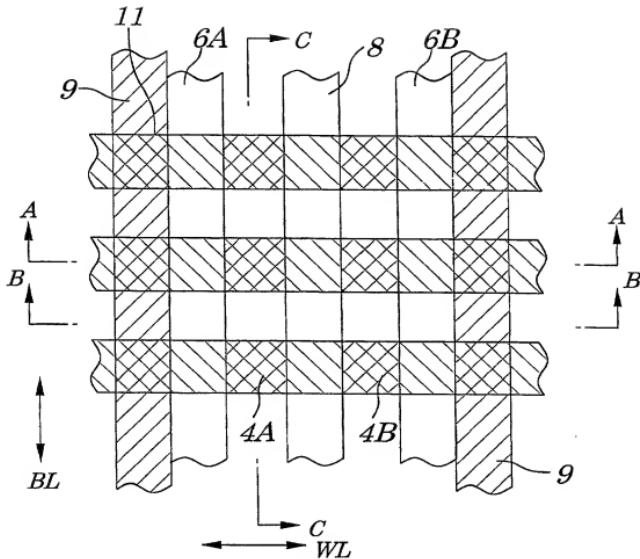
FIG.23
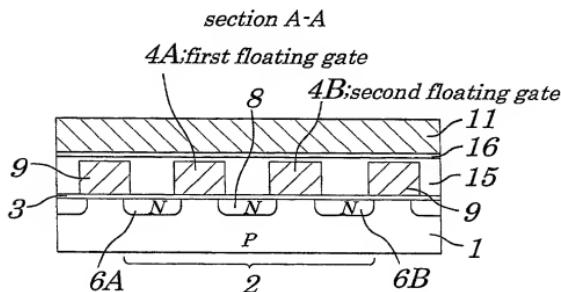
section B-B
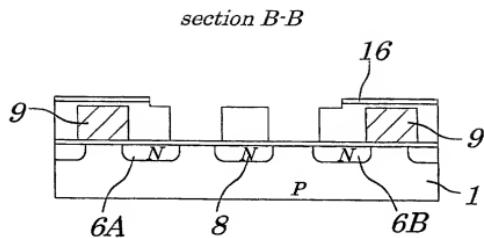
FIG.24
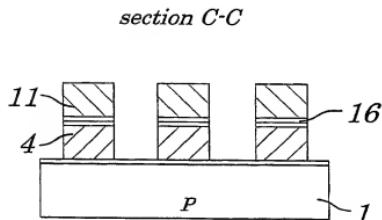
section C-C

FIG.25
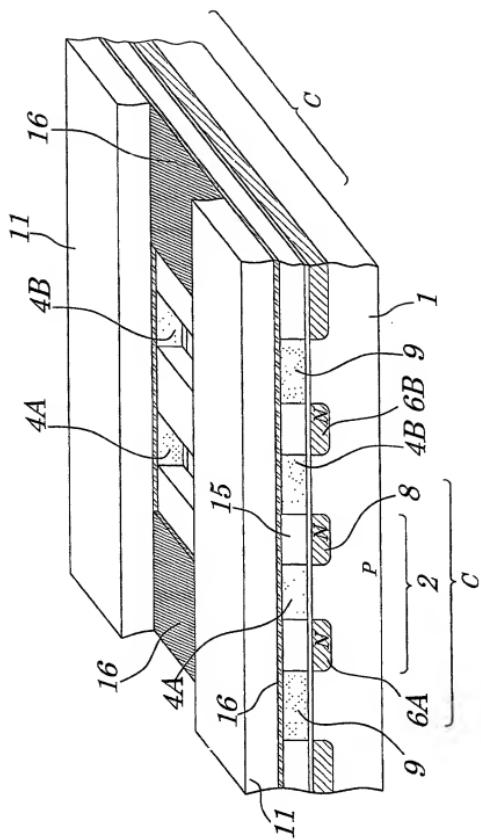
FIG.26
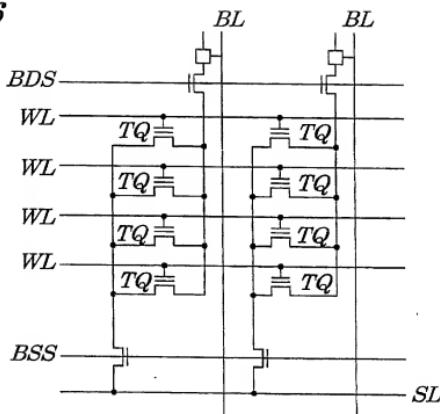
FIG.27
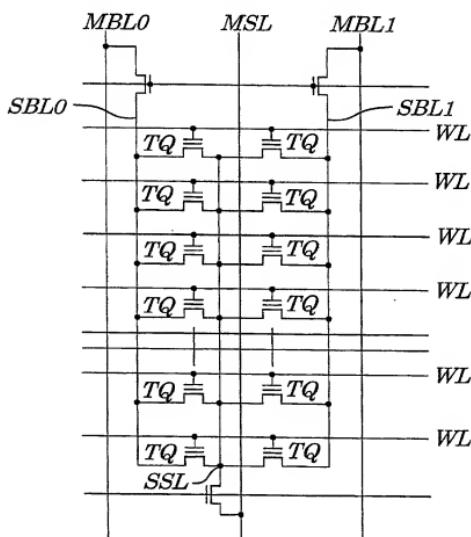
FIG.28
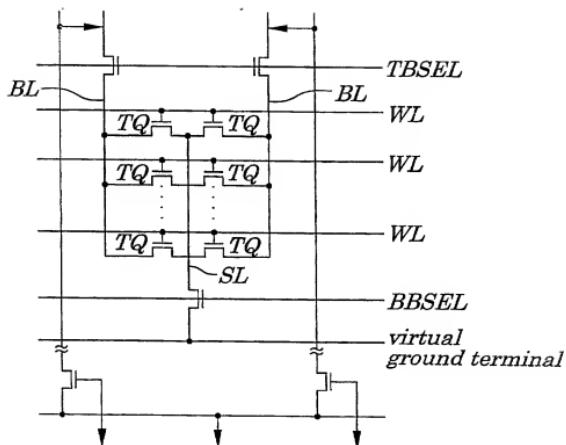

FIG.29
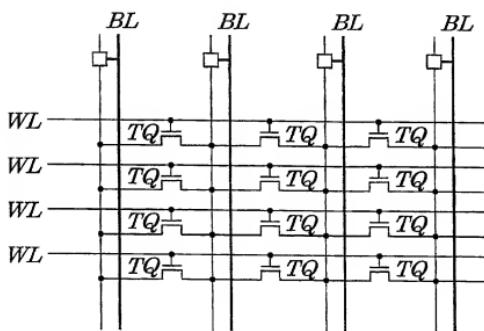
FIG.30 (PRIOR ART)
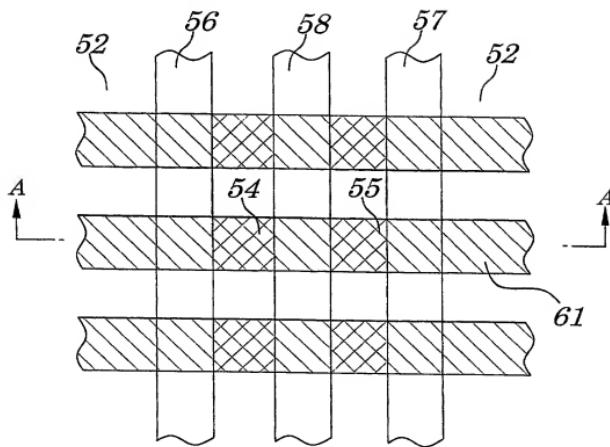

FIG.31 (PRIOR ART)
section A-A
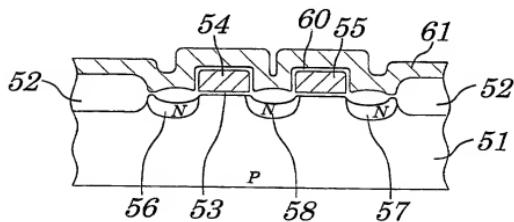
## FIG.32A (PRIOR ART)
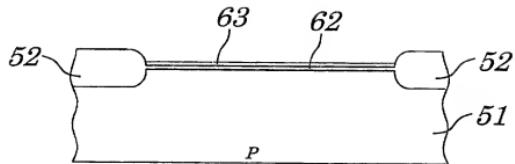
FIG.32B (PRIOR ART)
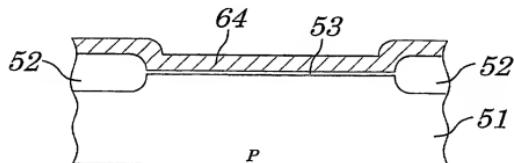
FIG.32C (PRIOR ART)
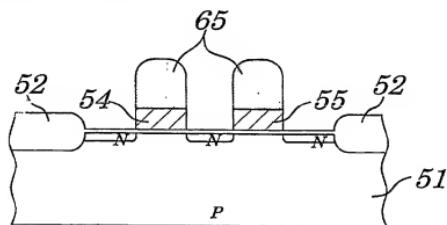
FIG.33A (PRIOR ART)
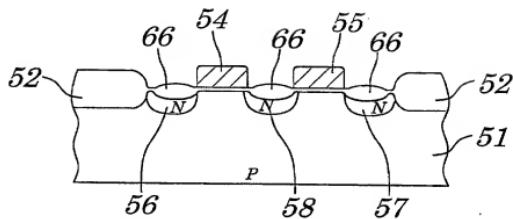
FIG.33B (PRIOR ART)

FIG.34 (PRIOR ART)